ROHS Compliance, The RF MOSFET Line, Enhancement Mode

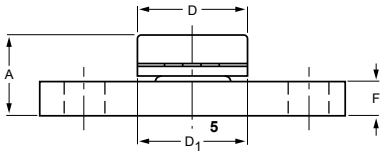
HG245B

Silicon MOS N-CHANNEL RF POWER TRANSISTOR

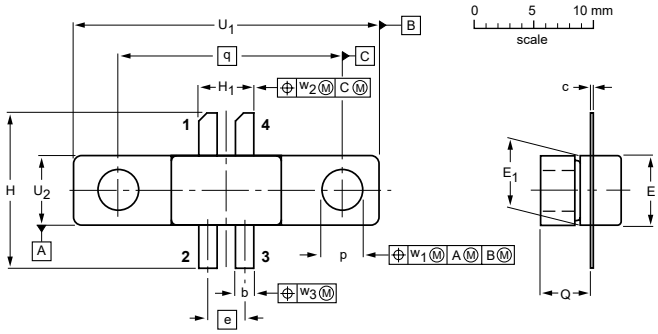
HG Semiconductors

DESCRIPTION

Silicon N-channel enhancement mode vertical D-MOS transistor designed for large signal amplifier applications up to 175 MHz frequency range.



1.Drain
2.Gate
3.Gate
4.Drain
5.Source



FEATURES

- Output Power: 30 W
- Power Gain: 14 dB Min@175M, 28V
- Efficiency: 55% Min

DIMENSIONS

UNIT	A	b	c	D	D_1	E	E_1	e	F	H	H_1	p	Q	q	U_1	U_2	w_1	w_2	w_3
mm	6.84 6.01	1.65 1.40	0.15 0.10	9.25 9.04	9.27 9.02	5.94 5.74	5.97 5.72	3.05	3.05 2.54	12.96 11.94	4.96 4.19	3.48 3.23	4.34 4.04	18.42	24.90 24.64	5.97 5.72	0.25	0.51	0.25
inches	0.269 0.237	0.065 0.055	0.006 0.004	0.364 0.356	0.365 0.355	0.234 0.226	0.235 0.225	0.120	0.120 0.100	0.510 0.470	0.195 0.165	0.137 0.127	0.171 0.159	0.725	0.980 0.970	0.235 0.225	0.010	0.020	0.010

MAXIMUM RATINGS

CHARACTERISTICS	SYMBOL	RATINGS	UNITS
Drain–Source Voltage	V_{DSS}	65	V
Gate–Source Voltage	V_{GS}	±20	V
Drain Current — Continuous	I_D	4.5	A
Total Device Dissipation	P_D	75	W
Junction Temperature	T_J	200	°C
Storage Temperature Range	T_{STG}	-65 to +150	°C

ELECTRICAL CHARACTERISTICS

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Drain–Source Breakdown Voltage	$V_{(BR)DSS}$	I_D=5mA,V_{GS}=0	65	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS}=0V,V_{DS}=28V	-	-	1	mAdc
Gate–Source Leakage Current	I_{GSS}	V_{GS}=±20V,V_{DS}=0V	-	-	1	uAdc
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = 10 V, I_D = 5mA	2.0	-	4.5	V
Drain-Source On-State Resistance	R_{Dson}	V_{DS} = 10 V, I_D = 0.75A	-	0.8	1.7	Ω
Forward Transconductance	gfs	V_{DS} = 10 V, I_D = 0.75A	600	850	-	mS
Input Capacitance	Ciss	V_{DS} = 28 V,V_{GS} = 0 V, f = 1.0 MHz	-	45	-	pF
Output Capacitance	Coss		-	38	-	pF
Reverse Transfer Capacitance	Crss		-	3.8	-	pF
Common Source Power Gain	G_P	V_{DD}=28V,P_{OUT}=30W, f=175MHz	14.0	-	-	dB
Drain Efficiency	η_D		55	-	-	%

Note : Above parameters , ratings , limits and conditions are subject to change.